Examiner Interview Summary

A telephonic interview was conducted on November 12, 2008 with Examiner Petranek and the Applicants' undersigned representative. Applicants' undersigned representative discussed independent Claims 1, 5 and 10 and the cited reference Larsen et al., (US Pat No. 5,115,500) (hereinafter Larsen). Examiner Petranek indicated that the claims would overcome Larsen by amendment to further clarify that the concatenation of a first plurality of bits of the address to the instruction and concatenation of a second plurality of bits of the address to the instruction resulting in different meanings to a same processor. As such, Applicants have respectfully amended independent Claims 1, 5 and 10 to further clarify this aspect of the invention.

Rejections 35 U.S.C. §103

Claims 1-3, 5-7, 9-12 and 14 are rejected, under 35 U.S.C. §103(a), as being allegedly unpatentable by Larsen et al, (US Pat No. 5,115,500) (hereinafter Larsen). Applicants respectfully traverse in view of the following.

Independent Claim 1 recites:

"fetching an instruction using a corresponding address from a memory unit, wherein a first meaning is associated with the instruction stored at the corresponding address by a same processor when a first plurality of bits from the corresponding address is concatenated with the instruction, and wherein a second meaning is associated with the instruction stored at the corresponding address by the same processor when a second plurality of bits from the corresponding address is concatenated with the instruction."

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As presented above and as agreed upon during the Examiner Interview, the above recited limitation overcomes the Larsen reference. Larsen discloses storing incompatible machine languages for two or more different machine types (see Larsen, col. 4, lines 58-64) by storing incompatible languages in various portions of segregated locations of the I-store (see Larsen, col. 5, lines 4-7). For example, an instruction identified by the three high order address bits "111" are decoded according to "type 2" decode rule whereas other address bits are decoded according to "type 1" (see Larsen, col. 6, lines 30-40).

As a result, an instruction stored in a location has only one type. Associating the instruction with a different type requires the instruction to be stored in a different location of a memory component. As such, Larsen fails to teach or suggest fetching an instruction using a corresponding address from a memory unit, wherein a first meaning is associated with the instruction stored at the corresponding address by a same processor when a first plurality of bits from the corresponding address is concatenated with the instruction, and wherein a second meaning is associated with the instruction stored at the corresponding address by the same processor when a second plurality of bits from the corresponding address is concatenated with the instruction, as claimed.

As presented and discussed above, Larsen discloses that an instruction stored at a given address has only one type. Thus, concatenating does not

TRAN-P072 Art Unit: 2183 US App. No.: 10/623,101 Examiner: Petranek, Jacob A extend the number of instructions, as disclosed by Larsen. The number of instruction, as disclosed by Larsen, is increased by storing the instruction in different locations. As such, Larsen fails to teach or suggest concatenating a portion of the corresponding address to the instruction to form an extended instruction, wherein the concatenation increases a number of instructions in an instruction set, as claimed.

Accordingly, Larsen fails to render independent Claim 1 obvious, under 35 U.S.C. §103(a). Independent Claims 5 and 10 recite limitations similar to that of independent Claim 1 and are patentable for similar reasons. Dependent claims are patentable by virtue of their dependency. As such, allowance of Claims 1-3, 5-7, 9-12 and 14 is earnestly solicited.

Claims 4, 8 and 13 are rejected, under 35 U.S.C. §103(a), as being allegedly unpatentable over Larsen in view of ("390 Principles of Operation") (hereinafter IBM). Claims 4, 8 and 13 depend from independent Claims 1, 5 and 10 respectively. IBM does not remedy the shortcomings of Larsen with respect to independent Claims 1, 5 and 10. Accordingly, Claims 4, 8 and 13 are patentable by virtue of their dependency and their allowance is earnestly solicited.

For the above reasons, the Applicants request reconsideration and withdrawal of the rejections of record.

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CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims 1-14 is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-14 are in condition for allowance.

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Respectfully submitted, MURABITO, HAO & BARNES LLP

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